METHOD OF FORMING GROOVE ISOLATION FILLED WITH DIELECTRIC FOR SEMICONDUCTOR DEVICE

This is a continuation of co-pending application Ser. No. 915,521 filed on Oct. 6, 1986.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method of forming a groove isolation filled with a dielectric material for a semiconductor device, more particularly to a method appicable for an integrated circuit which requires a high integration density, wherein the prior art has a problem the formation of a so-called BIRD'S BEAK or BIRD'S HEAD in forming a groove isolation, which limits the integration density. The method moreover has a special feature of forming isolation grooves by a self-alignment method.

With a need for higher integration density in semiconductor technology, various methods of isolatio have been introduced. A method relating to a pn-junction isolation has been utilized for a long time, but this method needs a comparatively large isolation region on a substrate. In order to increase an integration density, a selective oxidation method of isolation has been introduced, known as LOCOS or Isoplanar isolation and has been widely used.

In another method for obtaining still higher integration density, a groove (sometimes called a trench, depending on its shape) isolation filled with dielectric material has been introduced. The present invention relates to this type of isolation method.

2. Description of the Prior Art

The isolation method of forming a groove and filling it with a dielectric material such as polysilicon is well known. The shape of the groove is divided into a few types, a V shape type, a trench type having a groove of deep depth and narrow width, a combination type of V shape and deep trench, etc. For simplicity, hereinafter, the first type is called a V-groove, the second a U-groove, and the third a Y-groove.

V-groove is formed in a silicon substrate having a surface crystal index of orientation (**100**) utilizing a method of wet etching in alkali solution, a U-groove is formed utilizing a method of reactive ion etching. U-groove is suitable for forming a depper groove than a V-groove.

The method of forming V-groove isolation filled with dielectric in the prior art is explained briefly using FIGS. **1**(*a*) through **1**(*f*). FIG. **1**(*a*) shows a cross sectional view of a substrate **1**, which comprises a p^--type silicon base layer **1**, an n^+-type silicon buried layer **2**, and an n-type silicon epitaxial layer **3**, and is formed by conventional bipolar techniques. The substrate **1** has a surface index of orientation (**100**). A silicon oxide (SiO_2) layer **4** and a silicon nitride (Si_3N_4) layer **5** are formed on the silicon epitaxial layer **3**. Both layers **4** and **5** corresponding to a region **6** of a top area of the V-groove are selectively etched and removed.

When the substrate having the above crystal orientation is used, anisotropical etching is carried out using an alkali solution, such as potassium hydroxide (KOH), and a V-groove is formed, whereby silicon oxide layer **4** and silicon nitride layer **5** are used as etch masks. A V-shape groove **14** is then formed as shown in FIG. **1**(*b*).

When the dimension W in FIG. **1**(*a*) is defined as a width of the V-groove, then the depth D of the V-groove is determined by the following relation:

$$D=(\tfrac{1}{2})\times W\times\tan(54.7°)\approx 0.7\ W$$

The equation shows that the depth of the groove is smaller than the width W ofthe isolation region.

In FIG. **1**(*c*) a silicon oxide layer **7**, having a thickness of about 5,000 Angstroms is grown on an inside surface of the groove by thermal oxidation process, and thereafter polycrystalline silicon (polysilicon) **8** is grown on an entire surface of the substrate **1**, the groove being filled **093**rewith.

Polysilicon **8** is polished mechanically and chemically using the silicon nitride layer **5** as a stopper as shown in FIG. **1**(*d*).

The surface of the polysilicon **8** filling the V-groove is thermally oxidized forming a silicon oxide layer **9** of 5,000 to 8,000 Angstroms in thickness, as shown in FIG. **1**(*e*).

After the silicon nitride layer **5** is removed, the substrate having a planar surface covered with a silicon oxide layers **4** and **9**, and having a V-groove for isolation is formed as shown in FIG. **1**(*f*).

The method described above is used to form V-groove isolation. When a deep isolation forming a vertical narrow trench (U-groove) is needed, an anisotropic etching method of reactive ion etching is utilized, wherein a mixed gas of carbon tetrachloride ($CC1_4$) and oxygen (O_2) is used. In forming a U-groove, silicon crystal orientation (**100**) is not necessary as in the case of a V-groove above described. Other processes, except for the above etching process, are the same as those applied for the V-groove.

The method of forming grooves above causes the formation of BIRD'S BEAK or BIRD'S HEAD, which increases the integration density of semiconductor devices.

FIG. **2** is an enlarged cross sectional view of a V-groove just before the removing step of silicon nitride layer **5**. Three silicon oxide layers of first formed layer **4**, second formed layer **7** inside the V-groove, and third formed layer **9** from polysilicon are joined together at the peripheral region of the V-groove on the substrate.

Thickness of the silicon oxide at the joint projects vertically forming the so-called BIRD'S HEAD **21**, and the thickness of the fBIRD'S HEAD decrease in an outward lateral direction under silicon nitride layer **5** forming the so-called BIRD'S BEAK **22**. These phenomena are caused by the fact that the oxidation of silicon requires additional amounts of space approximately to the volume of initial silicon and that oxidation of silicon has different characteristics depending on the material such as silicon substrate or polysilicon, and oxidation conditions thereof. The silicon and polysilicon, which forms the peripheral region of the V-groove, is most subjected to the oxidation process. Therefore, the volume of the silicon oxide increases vertically and laterally the shape thereof is deformed irregularly. This is almost the same in the case of forming a U-groove.

As explained above, the method of forming groove isolation filled with dielectric in the prior art has an important drawback of injuring the flatness of the substrate surface and substantially increasing the width of the groove isolation. This results in requiring more tolerance in subsequent mask alignment processes, limit-